

# NCV8770

## LDO Regulator - Ultra Low $I_q$ , Reset

### 350 mA

The NCV8770 is 350 mA LDO regulator with integrated reset functions dedicated for microprocessor applications. Its robustness allows NCV8770 to be used in severe automotive environments. Ultra low quiescent current as low as 21  $\mu\text{A}$  typical makes it suitable for applications permanently connected to battery requiring ultra low quiescent current with or without load. This feature is especially critical when modules remain in active mode when ignition is off. The NCV8770 contains protection functions as current limit, thermal shutdown and reverse output current protection.

#### Features

- Output Voltage Options: 5 V
- Output Voltage Accuracy:  $\pm 1.5\%$  ( $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ )
- Output Current up to 350 mA
- Ultra Low Quiescent Current: typ 21  $\mu\text{A}$  (max 28  $\mu\text{A}$ )
- Very Wide Range of  $C_{out}$  and ESR Values for Stability
- Microprocessor Compatible Control Functions:
  - Reset with Adjustable Power-On Delay
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features
  - Current Limitation
  - Thermal Shutdown
- These are Pb-Free Devices

#### Typical Applications

- Body Control Module
- Instruments and Clusters
- Occupant Protection and Comfort
- Powertrain

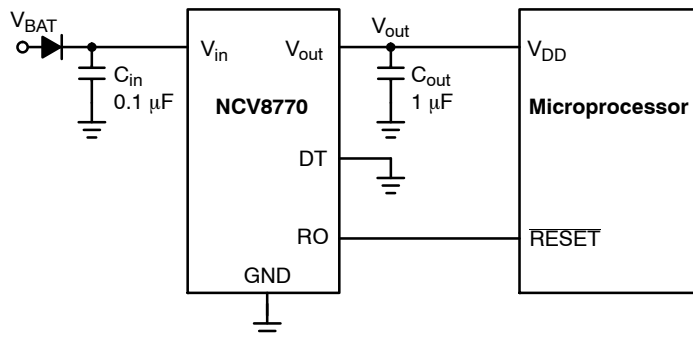


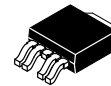
Figure 1. Typical Application Schematic



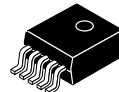
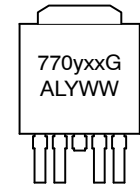
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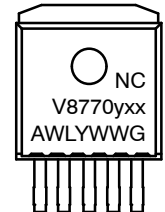
#### MARKING DIAGRAMS



DPAK-5  
DT SUFFIX  
CASE 175AA



D2PAK-5  
D5S SUFFIX  
CASE 936A



- y = Timing and Reset Threshold Option
- xx = Voltage Option
- A = Assembly Location
- WL, L = Wafer Lot
- Y = Year
- WW = Work Week
- G or ■ = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

# NCV8770

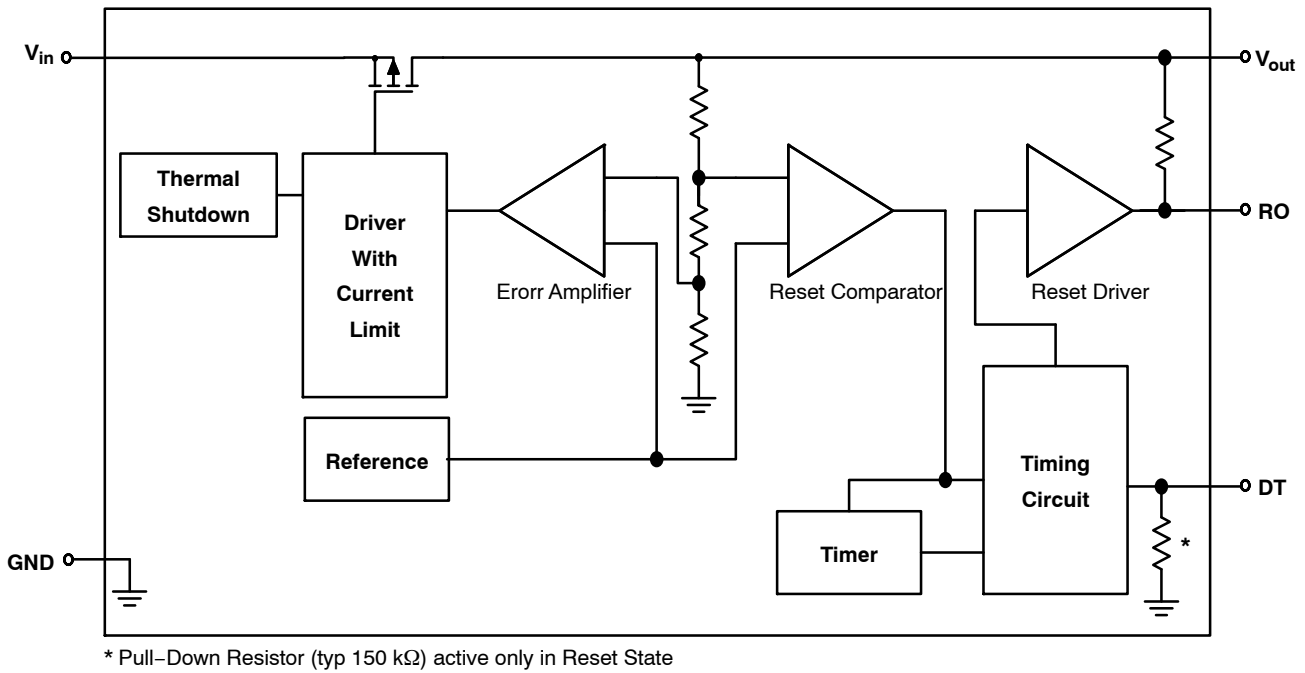


Figure 2. Simplified Block Diagram

## PIN CONNECTIONS



Figure 3. Pin Connections

## PIN FUNCTION DESCRIPTION

Pin No. DPAK-5 D2PAK-5	Pin Name	Description
1	$V_{in}$	Positive Power Supply Input. Connect 0.1 $\mu$ F capacitor to ground.
2	RO	Reset Output. 30 k $\Omega$ internal Pull-up resistor connected to $V_{out}$ . RO goes Low when $V_{out}$ drops by more than 7% (typ) from its nominal value (for NCV8770y devices with y = 1,2,3,...) or more than 10% (typ) from its nominal value (for NCV8770y devices with y = A, B, C,...).
3, TAB	GND	Power Supply Ground.
4	DT	Reset Delay Time Select. Short to GND or connected to $V_{out}$ to select time.
5	$V_{out}$	Regulated Output Voltage. Connect 1 $\mu$ F capacitor with ESR < 100 $\Omega$ to ground.
-	NC	Not Connected
-	GND	Exposed Pad is Connected to Ground.

**ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 1) DC Transient, t < 100 ms	V <sub>in</sub>	-0.3 -	40 45	V
Input Current	I <sub>in</sub>	-5	-	mA
Output Voltage (Note 2)	V <sub>out</sub>	-0.3	5.5	V
Output Current	I <sub>out</sub>	-3	Current Limited	mA
DT (Reset Delay Time Select) Voltage	V <sub>DT</sub>	-0.3	5.5	V
DT (Reset Delay Time Select) Current	I <sub>DT</sub>	-1	1	mA
Reset Output Voltage	V <sub>RO</sub>	-0.3	5.5	V
Reset Output Current	I <sub>RO</sub>	-3	3	mA
Junction Temperature	T <sub>J</sub>	-40	150	°C
Storage Temperature	T <sub>STG</sub>	-55	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. 5.5 V or (V<sub>in</sub> + 0.3 V) (whichever is lower).

**ESD CAPABILITY** (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD <sub>HBM</sub>	-2	2	kV
ESD Capability, Machine Model	ESD <sub>MM</sub>	-200	200	V
ESD Capability, Charged Device Model	ESD <sub>CDM</sub>	-1	1	kV

3. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002 (JS-001-2010)  
 ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)  
 ESD Charge Device Model tested per AEC-Q100-011 (EIA/JESD22-C101)

**LEAD SOLDERING TEMPERATURE AND MSL** (Note 4)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level DPAK-5 D2PAK-5	MSL		1 1	-
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions	T <sub>SLD</sub>	-	265 peak	°C

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**THERMAL CHARACTERISTICS** (Note 5)

Rating	Symbol	Value	Unit
Thermal Characteristics, DPAK-5 Thermal Resistance, Junction-to-Air (Note 6) Thermal Reference, Junction-to-Case (Note 6)	R <sub>θJA</sub> R <sub>ψJC</sub>	56 8.4	°C/W
Thermal Characteristics, D2PAK-5 Thermal Resistance, Junction-to-Air (Note 6) Thermal Reference, Junction-to-Case (Note 6)	R <sub>θJA</sub> R <sub>ψJC</sub>	53 8.4	°C/W

5. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
6. Values based on copper area of 645 mm<sup>2</sup> (or 1 in<sup>2</sup>) of 1 oz copper thickness and FR4 PCB substrate.

**RECOMMENDED OPERATING RANGE** (Note 7)

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 8)	V <sub>in</sub>	5.5	40	V
Junction Temperature	T <sub>J</sub>	-40	150	°C

7. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
8. Minimum V<sub>in</sub> = 5.5 V or (V<sub>out</sub> + V<sub>DO</sub>), whichever is higher.

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**ELECTRICAL CHARACTERISTICS**  $V_{in} = 13.2\text{ V}$ ,  $C_{in} = 0.1\ \mu\text{F}$ ,  $C_{out} = 1\ \mu\text{F}$ , for typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; unless otherwise noted. (Notes 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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## REGULATOR OUTPUT

Output Voltage (Accuracy %)	$T_J = 25^\circ\text{C}$ to $125^\circ\text{C}$ $V_{in} = 5.575\text{ V}$ to $16\text{ V}$ , $I_{out} = 0.1\text{ mA}$ to $200\text{ mA}$	$V_{out}$	4.925 (-1.5 %)	5.0	5.075 (+1.5%)	V
Output Voltage (Accuracy %)	$V_{in} = 5.6\text{ V}$ to $40\text{ V}$ , $I_{out} = 0.1\text{ mA}$ to $200\text{ mA}$ $V_{in} = 5.975\text{ V}$ to $16\text{ V}$ , $I_{out} = 0.1\text{ mA}$ to $350\text{ mA}$	$V_{out}$	4.9 4.9 (-2 %)	5.0 5.0	5.1 5.1 (+2%)	V
Output Voltage (Accuracy %)	$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ $V_{in} = 5.975\text{ V}$ to $28\text{ V}$ , $I_{out} = 0\text{ mA}$ to $350\text{ mA}$	$V_{out}$	4.9 (-2 %)	5.0	5.1 (+2%)	V
Line Regulation	$V_{in} = 6\text{ V}$ to $28\text{ V}$ , $I_{out} = 5\text{ mA}$	$Reg_{line}$	-20	0	20	mV
Load Regulation	$I_{out} = 0.1\text{ mA}$ to $350\text{ mA}$	$Reg_{load}$	-35	0	35	mV
Dropout Voltage (Note 11)	$I_{out} = 200\text{ mA}$ $I_{out} = 350\text{ mA}$	$V_{DO}$	- -	250 440	500 875	mV

## QUIESCENT CURRENT

Quiescent Current ( $I_q = I_{in} - I_{out}$ )	$I_{out} = 0.1\text{ mA}$ , $T_J = 25^\circ\text{C}$ $I_{out} = 0.1\text{ mA}$ to $350\text{ mA}$ , $T_J \leq 125^\circ\text{C}$	$I_q$	- -	21 -	27 28	$\mu\text{A}$
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## CURRENT LIMIT PROTECTION

Current Limit	$V_{out} = 0.96 \times V_{out\_nom}$	$I_{LIM}$	400	-	1100	mA
Short Circuit Current Limit	$V_{out} = 0\text{ V}$	$I_{SC}$	400	-	1100	mA

## PSRR

Power Supply Ripple Rejection (Note 12)	$f = 100\text{ Hz}$ , $0.5\ V_{pp}$	PSRR	-	54	-	dB
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## DT (RESET DELAY TIME SELECT)

DT Threshold Voltage Logic Low Logic High		$V_{th(DT)}$	- 2.0	- -	0.8 -	V
DT Input Current	$V_{DT} = 5\text{ V}$	$I_{DT}$	-	-	1.0	$\mu\text{A}$

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_A \approx T_J$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

11. Measured when output voltage falls 100 mV below the regulated voltage at  $V_{in} = 13.2\text{ V}$ .

12. Values based on design and/or characterization.

13. See APPLICATION INFORMATION section for Reset Thresholds and Reset Delay Time Options

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**ELECTRICAL CHARACTERISTICS**  $V_{in} = 13.2\text{ V}$ ,  $C_{in} = 0.1\ \mu\text{F}$ ,  $C_{out} = 1\ \mu\text{F}$ , for typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; unless otherwise noted. (Notes 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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## RESET OUTPUT RO

Output Voltage Reset Threshold (Note 13) (NCV8770y) where y = 1,2,3,... 5.0 V (NCV8770y) where y = A,B,C,... 5.0 V	$V_{out}$ decreasing, $V_{in} > 5.5\text{ V}$	$V_{RT}$	90 87	93 90	96 93	% $V_{out}$
Reset Hysteresis		$V_{RH}$	–	2.0	–	% $V_{out}$
Maximum Reset Sink Current	$V_{out} = 4.5\text{ V}$ , $V_{RO} = 0.25\text{ V}$	$I_{ROmax}$	1.75	–	–	mA
Reset Output Low Voltage	$V_{out} > 1\text{ V}$ , $I_{RO} < 200\ \mu\text{A}$	$V_{ROL}$	–	0.15	0.25	V
Reset Output High Voltage		$V_{ROH}$	4.5	–	–	V
Integrated Reset Pull-up Resistor		$R_{RO}$	15	30	50	k $\Omega$
Reset Delay Time (Note 13)	Min Available Time, DT connected to GND Max Available Time, DT connected to $V_{out}$	$t_{RD}$	3.2 102.4 –20%	4.0 128	4.8 153.6 +20%	ms
Reset Reaction Time (see Figure 21)		$t_{RR}$	16	25	38	$\mu\text{s}$

## THERMAL SHUTDOWN

Thermal Shutdown Temperature (Note 12)		$T_{SD}$	150	175	195	$^\circ\text{C}$
Thermal Shutdown Hysteresis (Note 12)		$T_{SH}$	–	25	–	$^\circ\text{C}$

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_A \approx T_J$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

11. Measured when output voltage falls 100 mV below the regulated voltage at  $V_{in} = 13.2\text{ V}$ .

12. Values based on design and/or characterization.

13. See APPLICATION INFORMATION section for Reset Thresholds and Reset Delay Time Options

TYPICAL CHARACTERISTICS

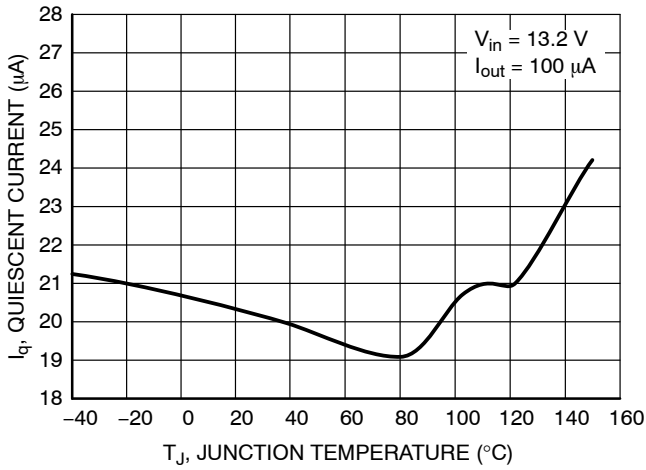


Figure 4. Quiescent Current vs. Temperature

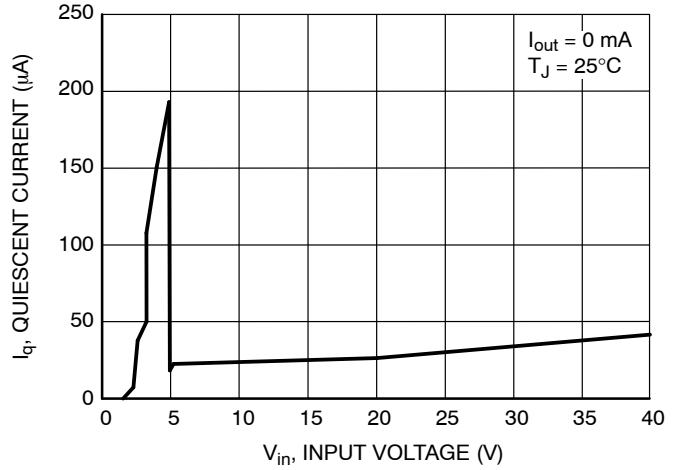


Figure 5. Quiescent Current vs. Input Voltage

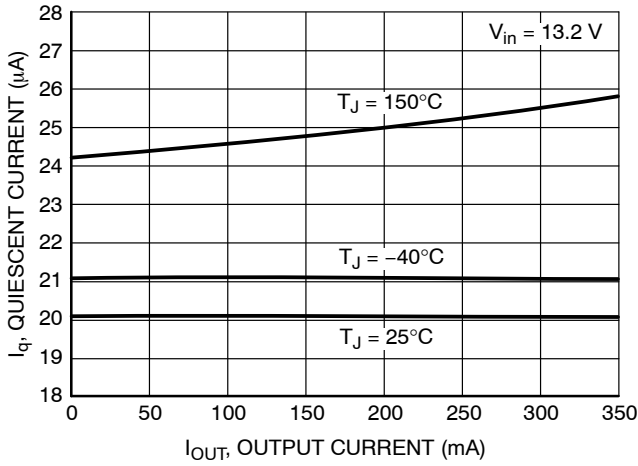


Figure 6. Quiescent Current vs. Output Current

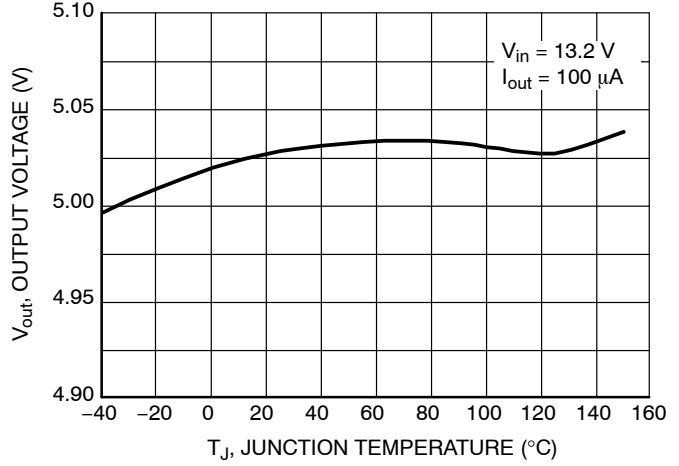


Figure 7. Output Voltage vs. Temperature

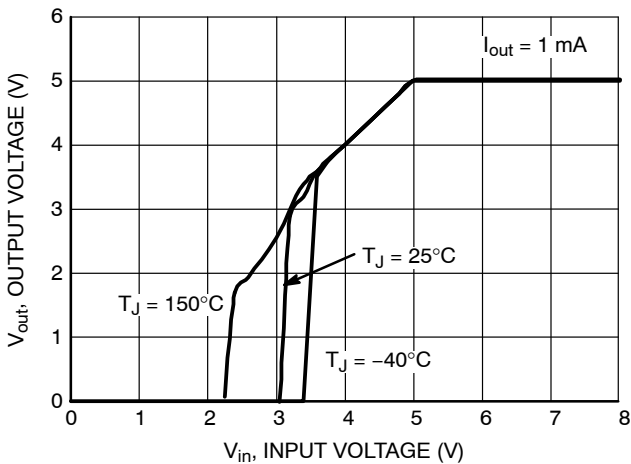


Figure 8. Output Voltage vs. Input Voltage

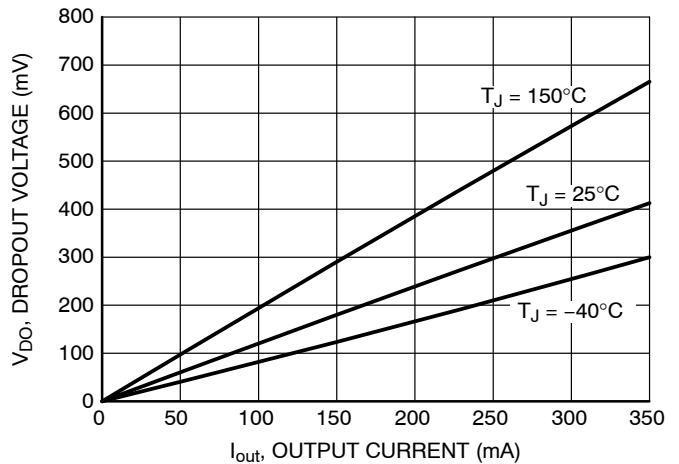


Figure 9. Dropout vs. Output Current

TYPICAL CHARACTERISTICS

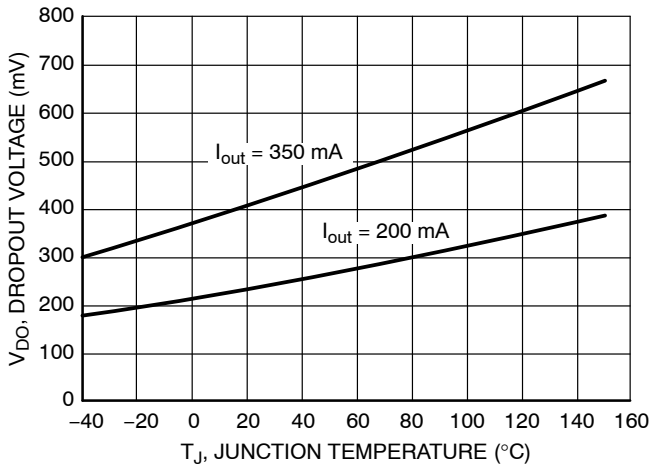


Figure 10. Dropout vs. Temperature

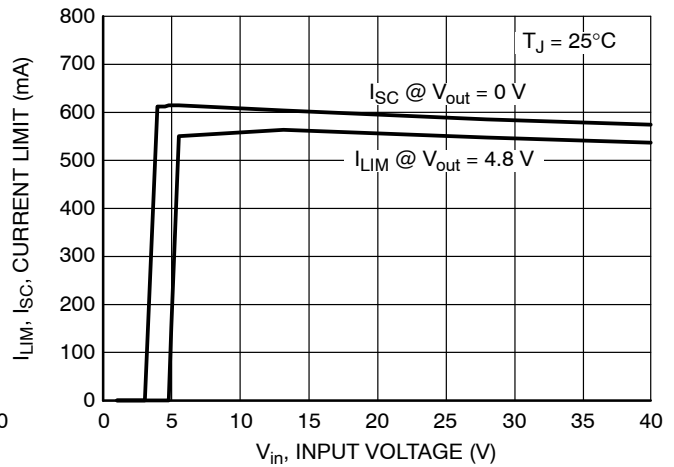


Figure 11. Output Current Limit vs. Input Voltage

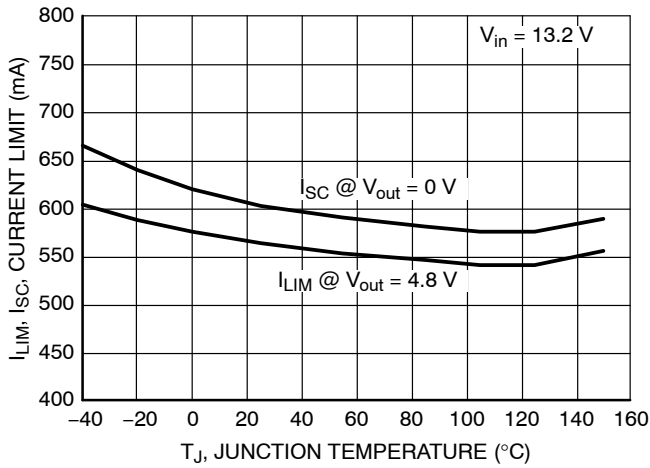


Figure 12. Output Current Limit vs. Temperature

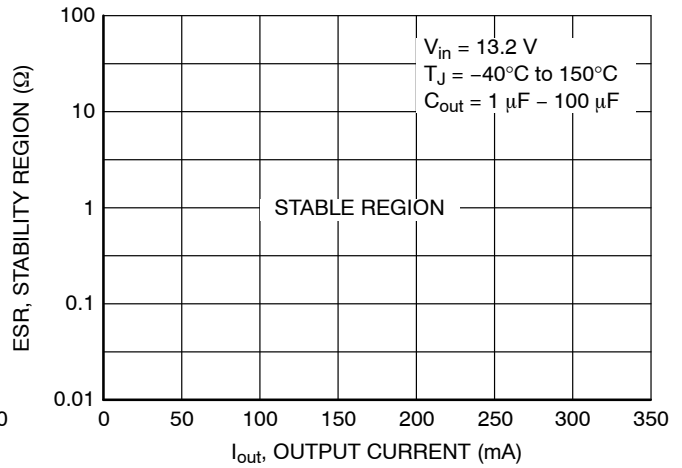


Figure 13.  $C_{out}$  ESR Stability Region vs. Output Current

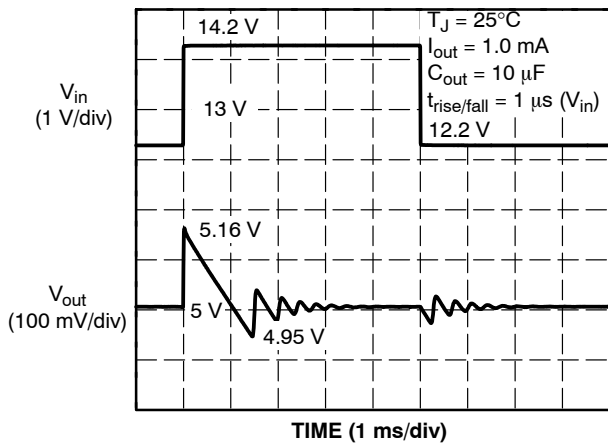


Figure 14. Line Transients

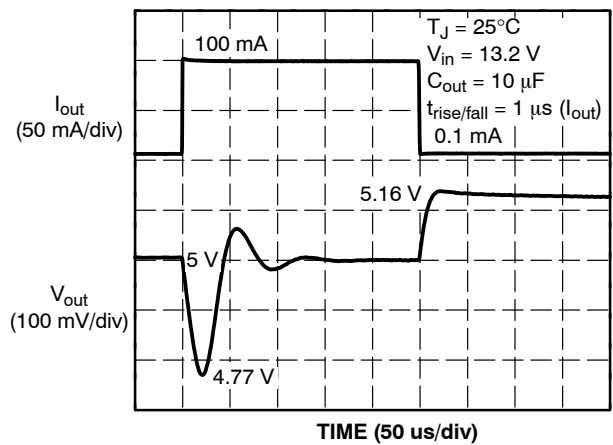


Figure 15. Load Transients

TYPICAL CHARACTERISTICS

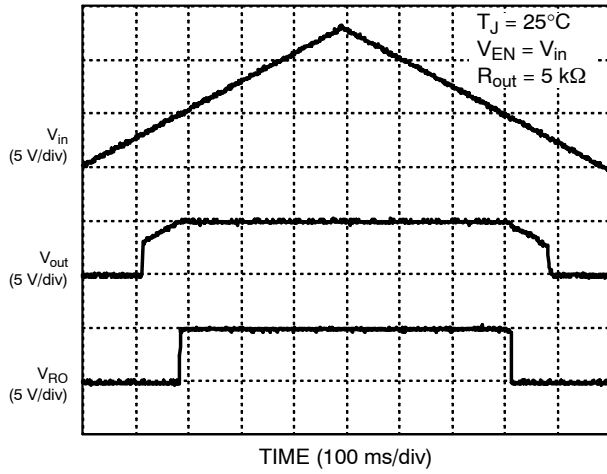


Figure 16. Power Up/Down Response

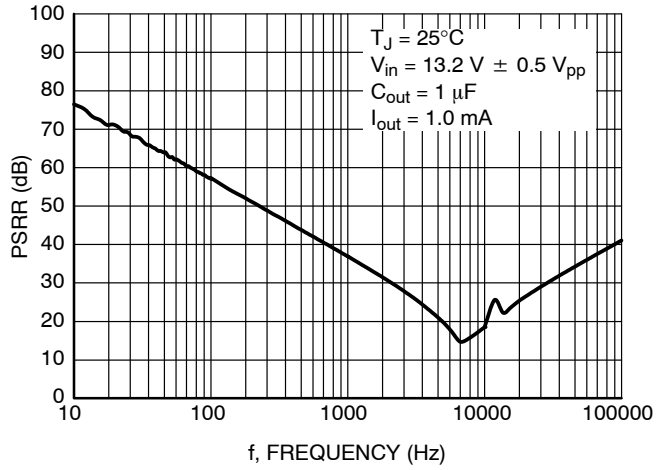


Figure 17. PSRR vs. Frequency

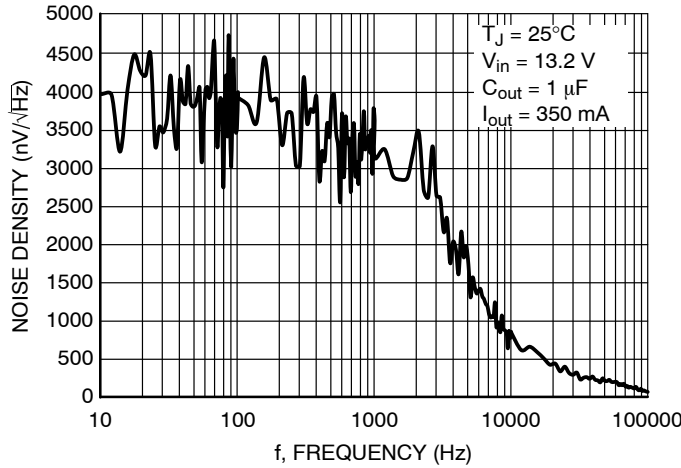


Figure 18. Noise vs. Frequency

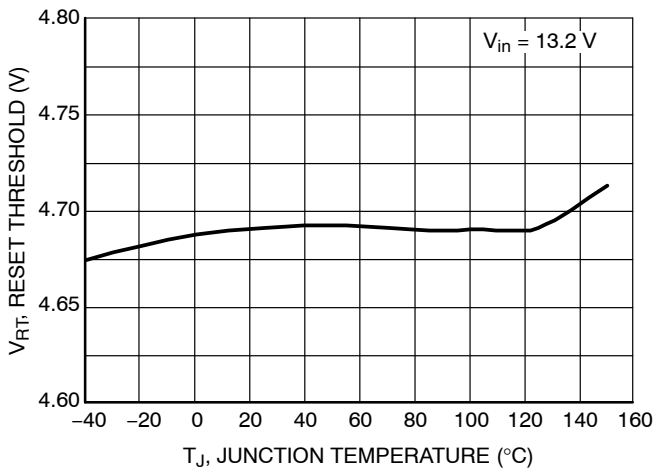


Figure 19. Reset Threshold vs. Temperature

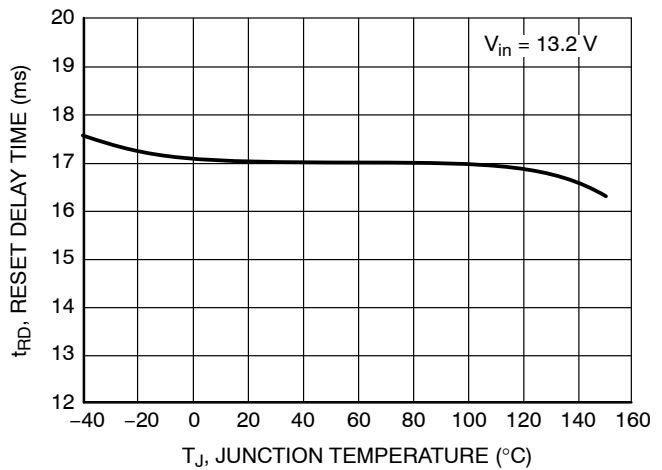


Figure 20. Reset Delay Time vs. Temperature

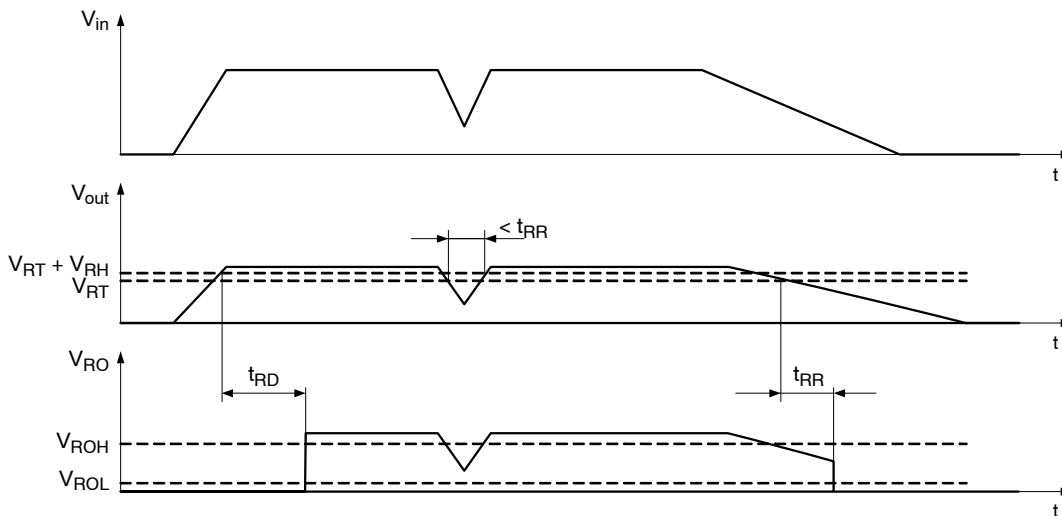


Figure 21. Reset Function and Timing Diagram

**DEFINITIONS**

**General**

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

**Output voltage**

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

**Line Regulation**

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

**Load Regulation**

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

**Dropout Voltage**

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

**Quiescent Current**

Quiescent Current ( $I_q$ ) is the difference between the input current (measured through the LDO input pin) and the output load current.

**Current Limit and Short Circuit Current Limit**

Current Limit is value of output current by which output voltage drops below 96% of its nominal value. Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

**PSRR**

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

**Line Transient Response**

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

**Load Transient Response**

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low-load and high-load conditions.

**Thermal Protection**

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

**Maximum Package Power Dissipation**

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV8770 regulator is self-protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figure 4 to Figure 21.

**Input Decoupling (C<sub>in</sub>)**

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV8770 package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

**Output Decoupling (C<sub>out</sub>)**

The NCV8770 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs Output Current is shown in Figure 13. The minimum output decoupling value is 1 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

**Reset Operation**

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. The timing diagram of reset function is shown in Figure 21. This is in the form of a logic signal on RO. Output voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to V<sub>out</sub> = 1.0 V. For 5 V voltage option, the Reset Output (RO) circuitry includes internal pull-up (30 kΩ) connected to the output (V<sub>out</sub>) No external pull-up is necessary.

**Reset Delay Time Select**

Selection of the NCV8770y devices and the state of the DT pin determines the available Reset Delay times. The part is designed for use with DT tied to ground or V<sub>out</sub>, but may be controlled by any logic signal which provides a threshold between 0.8 V and 2 V. The default condition for an open DT pin is the slower Reset time (DT = GND condition). Times are in pairs and are highlighted in the chart below. Consult factory for availability. The Delay Time select (DT) pin is logic level controlled and provides Reset Delay time per the chart. Note the DT pin is sampled only when RO is low, and changes to the DT pin when RO is high will not effect the reset delay time.

**RESET DELAY AND RESET THRESHOLD OPTIONS**

	DT = GND Reset Time	DT = V <sub>out</sub> Reset Time	Reset Threshold
NCV87701	8 ms	128 ms	93%
NCV87702	8 ms	32 ms	93%
NCV87703	16 ms	64 ms	93%
NCV87704	32 ms	128 ms	93%
NCV87705	4 ms	8 ms	93%
NCV87706	16 ms	128 ms	93%
NCV8770A	8 ms	128 ms	90%
NCV8770B	8 ms	32 ms	90%
NCV8770C	16 ms	64 ms	90%
NCV8770D	32 ms	128 ms	90%
NCV8770E	4 ms	8 ms	90%
NCV8770F	16 ms	128 ms	90%

NOTE: The timing values can be selected from the following list: 4, 8, 16, 32, 64, 128 ms. Contact factory for options not included in ORDERING INFORMATION table on following page.

**Thermal Considerations**

As power in the NCV8770 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8770 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8770 can handle is given by:

$$P_{D(max)} = \frac{[T_{J(max)} - T_A]}{R_{\theta JA}} \quad (eq. 1)$$

Since T<sub>J</sub> is not recommended to exceed 150°C, then the NCV8770 soldered on 645 mm<sup>2</sup>, 1 oz copper area, FR4 can dissipate up to 2.35 W (for D2PAK-5) when the ambient temperature (T<sub>A</sub>) is 25°C. See Figure 22 for R<sub>θJA</sub> versus PCB area. The power dissipated by the NCV8770 can be calculated from the following equations:

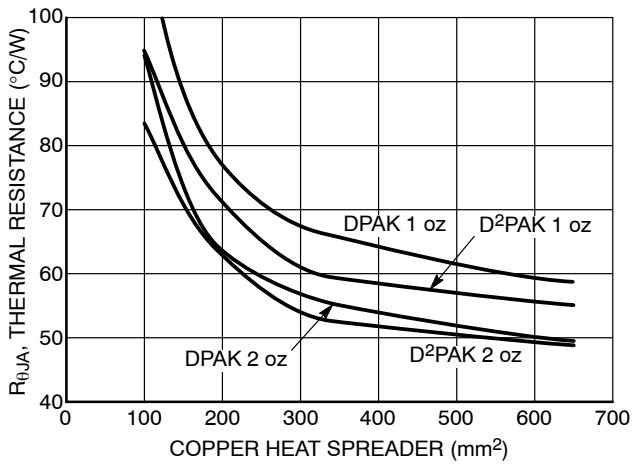
$$P_D = V_{in}(I_q@I_{out}) + I_{out}(V_{in} - V_{out}) \quad (eq. 2)$$

or

$$V_{in(max)} = \frac{P_{D(max)} + (V_{out} \times I_{out})}{I_{out} + I_q} \quad (eq. 3)$$

NOTE: Items containing I<sub>q</sub> can be neglected if I<sub>out</sub> >> I<sub>q</sub>.

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**Figure 22. Thermal Resistance vs. PCB Copper Area**

### Hints

$V_{in}$  and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8770 and make traces as short as possible.

### ORDERING INFORMATION

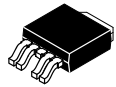
Device	Output Voltage	Reset Delay Time (DT = GND/ $V_{out}$ )	Reset Threshold	Marking	Package	Shipping <sup>†</sup>
NCV87706DT50RKG	5.0 V	16/128 ms	93%	770650G	DPAK-5 (Pb-Free)	2500 / Tape & Reel
NCV87706DS50R4G	5.0 V	16/128 ms	93%	NC V8770650	D2PAK-5 (Pb-Free)	800 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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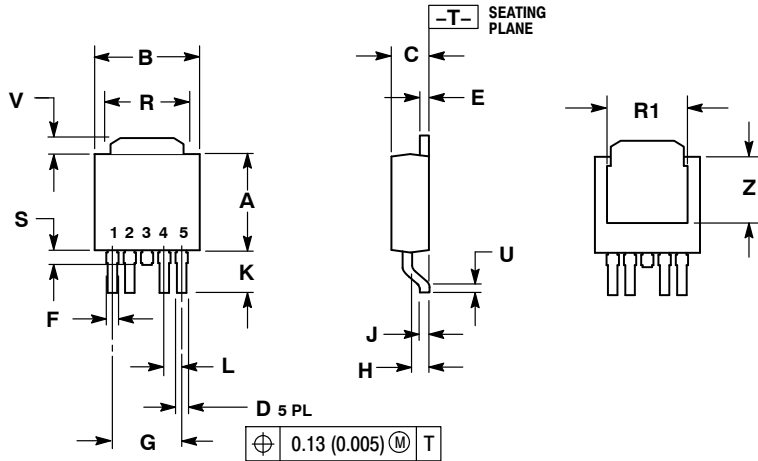
### DPAK-5, CENTER LEAD CROP

#### CASE 175AA

#### ISSUE B

DATE 15 MAY 2014

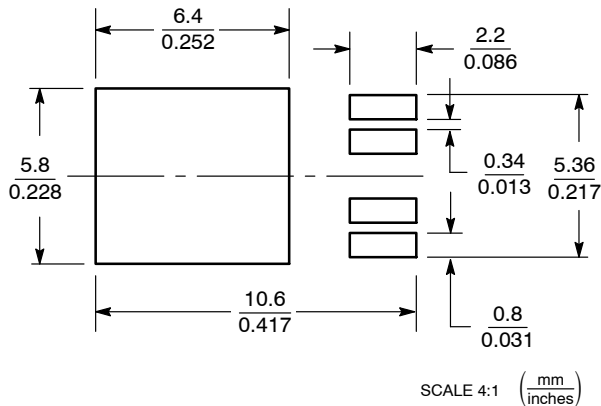
SCALE 1:1



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.

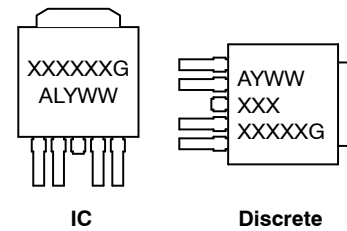
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAMS\*



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

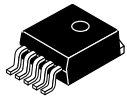
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<b>DESCRIPTION:</b>	<b>DPAK-5 CENTER LEAD CROP</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

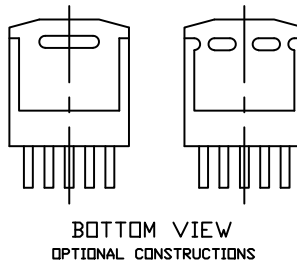
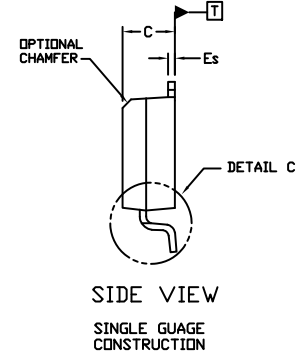
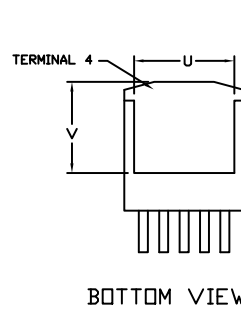
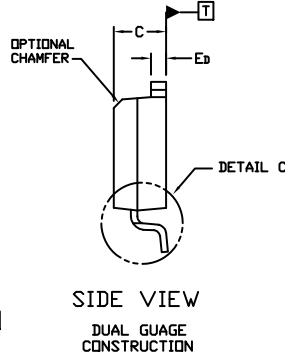
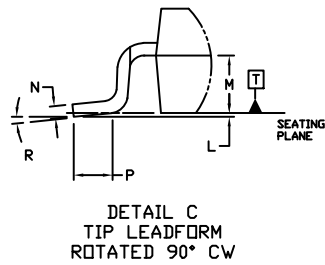
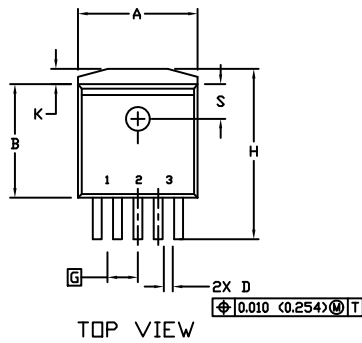
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### D<sup>2</sup>PAK 5-LEAD CASE 936A-02 ISSUE E

DATE 28 JUL 2021

SCALE 1:1

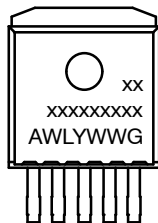


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

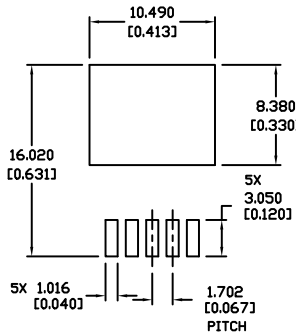
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.396	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
Ed	0.045	0.055	1.143	1.397
Es	0.018	0.026	0.457	0.660
G	0.067	BSC	1.702	BSC
H	0.539	0.579	13.691	14.707
K	0.050	REF	1.270	REF
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116	REF	2.946	REF
U	0.200	MIN	5.080	MIN
V	0.250	MIN	6.350	MIN

### GENERIC MARKING DIAGRAM\*



- xxxxxx = Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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